CLAIMS

1. A processor, comprising:

a first register configured to store one or more hardware-debug-test (HDT) enable bits;

a first control logic coupled to receive a plurality of HDT input signals, wherein the first control logic is coupled to access the first register; and

a second control logic coupled to the first register, wherein the second control logic is configured to store one or more default values in the first register in response to a reset of the processor.

2. The processor of claim 1, wherein the first control logic is further configured to receive a request to enter an HDT mode, wherein the first control logic is further configured to read selected entries of the one or more HDT enable bits stored in the first register in response to the request to enter HDT mode, and wherein the first control logic is further configured to grant or deny the request to enter HDT mode based on the selected entries of the one or more HDT enable bits.

3. The processor of claim 1, further comprising:

one or more non-volatile memory cells configured to store the one or more default values for the one or more HDT enable bits.

4. The processor of claim 3, wherein the second control logic is further coupled to read the one or more default values for the one or more HDT enable bits from the one or more non-volatile memory cells and to write the one or more default values for the one or more HDT enable bits into the first register in response to the reset of the processor.

5. The processor of claim 1, wherein the second control logic is further coupled to receive a signal indicative of the one or more default values for the one or more HDT enable bits and to write the one or more default values for the one or more HDT enable bits into the first register in response to the reset of the processor.

6. The processor of claim 1, wherein the second control logic is coupled to receive a RESET signal in response to the reset of the processor.

7. The processor of claim 1, further comprising:

a third register configured to store one or more microcode loader enable bits;

a third control logic coupled to receive a plurality of microcode inputs, wherein the third control logic is coupled to access the third register; and

a fourth control logic coupled to the third register, wherein the fourth control logic is configured to store one or more default values in the third register in response to a reset of the processor.

8. The processor of claim 7, wherein the third control logic is further configured to receive a request to modify microcode, wherein the third control logic is further configured to read selected entries of the

one or more microcode loader enable bits stored in the third register in response to the request to modify microcode, and wherein the third control logic is further configured to grant or deny the request to modify microcode based on the selected entries of the one or more microcode loader enable bits.

9. The processor of claim 1, further comprising:

a second register coupled to the first control logic, wherein the second register is configured to store one or more HDT enable lock bits.

10. The processor of claim 9, wherein the first control logic is further configured to receive a request to modify HDT mode status, wherein the first control logic is further configured to read selected entries in the one or more HDT enable lock bits stored in the second register in response to the request to modify HDT mode status, and wherein the first control logic is further configured to grant or deny the request to modify HDT mode based on the selected entries in the one or more HDT enable lock bits.

11. The processor of claim 9, wherein the first register and the second register are unified into a single register configured to store two or more bits, including one or more HDT enable bits and one or more HDT enable lock bits

12. The processor of claim 9, further comprising:

a third register configured to store one or more microcode loader enable bits;

a third control logic coupled to receive a plurality of microcode inputs, wherein the third control logic is coupled to access the third register; and

a fourth control logic coupled to the third register, wherein the fourth control logic is configured to store one or more default values in the third register in response to a reset of the processor.

13. The processor of claim 12, wherein the third control logic is further configured to receive a request to modify microcode, wherein the third control logic is further configured to read selected entries in the one or more microcode loader enable bits stored in the third register in response to the request to modify microcode, and wherein the third control logic is further configured to grant or deny the request to modify microcode based on the selected entries in the one or more microcode loader enable bits.

14. The processor of claim 12, wherein the second and fourth control logics are unified.

15. The processor of claim 14, wherein the first control logic, the second control logic, the third control logic, and the fourth control logic are unified.

16. A processor, comprising:

a first control logic coupled to receive a plurality of microcode inputs;

a first register coupled to the first control logic, wherein the first register is configured to store one or more microcode loader enable bits; and

a second control logic coupled to the first register, wherein the second control logic is configured to store one or more default values in the first register in response to a reset of the processor.

17. The processor of claim 16, wherein the first control logic is further configured to receive a request to modify microcode, wherein the first control logic is further configured to read selected entries of the one or more microcode loader enable bits stored in the first register in response to the request to modify microcode, and wherein the first control logic is further configured to grant or deny the request to modify microcode based on the selected entries of the one or more microcode loader enable bits.

18. The processor of claim 16, further comprising:

one or more non-volatile memory cells configured to store the one or more default values for the one or more microcode loader enable bits.

19. The processor of claim 18, wherein selected ones of the one or more non-volatile memory cells are configured to store the one or more default value for the one or more microcode loader enable bits.

20. The processor of claim 18, wherein the second control logic is further coupled to read the one or more default values for the one or more microcode loader enable bits from the one or more non-volatile memory cells and to write the one or more default values for the one or more microcode loader enable bits into the microcode loader register in response to the reset of the processor.

21. The processor of claim 16, wherein the second control logic is further coupled to receive a signal indicative of the one or more default values for the one or more microcode loader enable bits and to write the one or more default values for the one or more microcode loader enable bits into the first register in response to the reset of the processor.

22. The processor of claim 16, wherein the fourth control logic is coupled to receive a RESET signal in response to the reset of the processor.

23. The processor of claim 16, further comprising:

a second register coupled to the first control logic, wherein the second register is configured to store one or more microcode loader enable lock bits.

24. The processor of claim 23, wherein the first control logic is further configured to receive a request to modify microcode loader lock status, wherein the first control logic is further configured to read selected entries in the one or more microcode loader enable lock bits stored in the second register in response to the request to modify microcode loader lock status, and wherein the first control logic is further configured to grant or deny the request to modify microcode loader lock status based on the selected entries in the one or more microcode loader enable lock bits.

25. A method for determining an HDT mode enable status, the method comprising:
receiving a request to initiate the HDT mode;
determining HDT mode enable status;
initiating the HDT mode if the HDT mode enable status is set to enabled.

26. The method of claim 25, wherein determining HDT mode enable status comprises reading one or more entries corresponding to one or more HDT enable bits from a register.

27. A method for modifying microcode, the method comprising:
receiving a request to modify microcode;
determining microcode loader enable status;
modifying microcode if the microcode loader enable status is set to enabled.

28. The method of claim 27, wherein determining microcode loader enable status comprises reading one or more entries corresponding to one or more microcode loader enable bits from a register.

29. A method of changing HDT mode status, the method comprising:
receiving a request to change HDT mode status;
determining HDT mode enable lock status; and
modifying HDT mode status if the HDT mode enable lock status is set to unlocked.

30. The method of claim 29, wherein determining HDT mode enable lock status comprises reading one or more entries corresponding to one or more HDT enable lock bits from a register.

31. The method of claim 29, wherein modifying HDT mode status comprises writing one or more entries corresponding to one or more HDT enable bits to a register.

32. A method of changing microcode loader enable status, the method comprising:
receiving a request to change microcode loader enable status;
determining microcode loader enable lock status; and
modifying microcode loader enable status if the microcode loader enable lock status is set to unlocked.

33. The method of claim 32, wherein determining microcode loader enable lock status comprises reading one or more entries corresponding to one or more microcode loader enable lock bits from a register.

34. The method of claim 32, wherein modifying microcode loader enable status comprises writing one or more entries corresponding to one or more microcode loader enable bits to a register.

35. A method of operating a processor, the method comprising:

obtaining one or more default values, wherein obtaining the one or more default values is selected from the group consisting of:

reading the one or more default values from one or more non-volatile memory cells, and

receiving the one or more default values as a strapped value through a pull-up or pull-down resistor; and

writing the one or more default values as one or more various entries in one or more registers in response to a reset of the processor, wherein the one or more various entries are selected from the group consisting of:

one or more HDT enable bits,

one or more HDT enable lock bits,

one or more microcode loader enable bits, and

one or more microcode loader enable lock bits.

36. A processor, comprising:

means for receiving a request to initiate HDT mode;

means for determining HDT mode enable status; and

means for initiating HDT mode if the HDT mode status is set to enabled.

37. The processor of claim 36, further comprising:

means for storing an indication of the HDT mode status.

38. The processor of claim 37, further comprising:

means for providing the means for storing with one or more default values for the indication of the HDT mode status.

39. The processor of claim 38, further comprising:

means for receiving a request to change HDT mode status;

means for determining HDT mode lock status; and

means for modifying HDT mode status if the HDT mode lock status is set to unlocked.

40. The processor of claim 39, further comprising:

means for storing an indication of the HDT mode lock status.

41. A processor, comprising:

means for storing one or more default values, wherein the default values are selected from the group consisting of:

HDT enable status,

HDT enable lock status,

microcode loader enable status, and

microcode loader enable lock status;

means for obtaining the one or more default values, wherein obtaining the one or more default values is selected from the group consisting of:

reading the one or more default values from non-volatile memory, and

receiving the one or more default values as a strapped value through a pull-up or pull-down resistor; and

means for writing the one or more default values as one or more various entries in the means for storing the one or more default values in response to a reset of the processor, wherein the one or more various entries are selected from the group consisting of:

one or more HDT enable bits,

one or more HDT enable lock bits,

one or more microcode loader enable bits, and

one or more microcode loader enable lock bits.

42. A computer system, comprising:

a processor, comprising:

means for storing one or more default values, wherein the default values are selected from the group consisting of:

HDT enable status,

HDT enable lock status,

microcode loader enable status, and

microcode loader enable lock status;

means for obtaining the one or more default values, wherein obtaining the one or more default values is selected from the group consisting of:

reading the one or more default values from non-volatile memory, and

receiving the one or more default values as a strapped value through a pull-up or pull-down resistor; and

means for writing the one or more default values as one or more various entries in the means for storing the one or more default values in response to a reset of the processor, wherein the one or more various entries are selected from the group consisting of:

one or more HDT enable bits,

one or more HDT enable lock bits,

one or more microcode loader enable bits, and

one or more microcode loader enable lock bits;

a bridge coupled to the processor; and

a memory operably coupled to the processor, wherein the memory is configured to store BIOS code.

43. A computer readable program storage device encoded with instructions that, when executed by a computer system, performs a method of determining an HDT mode enable status, the method comprising:

receiving a request to initiate the HDT mode;

determining HDT mode enable status;
initiating the HDT mode if the HDT mode enable status is set to enabled.

44. The computer readable program storage device of claim 43, wherein determining HDT mode enable status comprises reading one or more entries corresponding to one or more HDT enable bits from a register.

45. A computer readable program storage device encoded with instructions that, when executed by a computer system, performs a method of modifying microcode, the method comprising:
receiving a request to modify microcode;
determining microcode loader enable status;
modifying microcode if the microcode loader enable status is set to enabled.

46. The computer readable program storage device of claim 45, wherein determining microcode loader enable status comprises reading one or more entries corresponding to one or more microcode loader enable bits from a register.

47. A computer readable program storage device encoded with instructions that, when executed by a computer system, performs a method of changing HDT mode status, the method comprising:
receiving a request to change HDT mode status;
determining HDT mode enable lock status; and
modifying HDT mode status if the HDT mode enable lock status is set to unlocked.

48. The computer readable program storage device of claim 47, wherein determining HDT mode enable lock status comprises reading one or more entries corresponding to one or more HDT enable lock bits from a register.

49. The computer readable program storage device of claim 47, wherein modifying HDT mode status comprises writing one or more entries corresponding to one or more HDT enable bits to a register.

50. A computer readable program storage device encoded with instructions that, when executed by a computer system, performs a method of changing microcode loader enable status, the method comprising:
receiving a request to change microcode loader enable status;
determining microcode loader enable lock status; and
modifying microcode loader enable status if the microcode loader enable lock status is set to unlocked.

51. The computer readable program storage device of claim 50, wherein determining microcode loader enable lock status comprises reading one or more entries corresponding to one or more microcode loader enable lock bits from a register.

52. The computer readable program storage device of claim 50, wherein modifying microcode loader enable status comprises writing one or more entries corresponding to one or more microcode loader enable bits to a register.

53. A computer readable program storage device encoded with instructions that, when executed by a computer system, performs a method of operating a processor, the method comprising:

obtaining one or more default values, wherein obtaining the one or more default values is selected from the group consisting of:

reading the one or more default values from one or more non-volatile memory cells, and

receiving the one or more default values as a strapped value through a pull-up or pull-down resistor; and

writing the one or more default values as one or more various entries in one or more registers in response to a reset of the processor, wherein the one or more various entries are selected from the group consisting of:

one or more HDT enable bits,

one or more HDT enable lock bits,

one or more microcode loader enable bits, and

one or more microcode loader enable lock bits.